**IN THE SPECIFICATION:**

**Paragraph beginning at line 3 of page 1 has been amended as follows:**

The present invention relates to a semiconductor memory device, and, more specifically, to ~~in particular,~~ an electrically rewritable nonvolatile semiconductor memory integrated circuit (electrically erasable programmable read only memory) (hereinafter, referred to as EEPROM). ~~Also, the~~ The invention also relates to a semiconductor memory device including a circuit having a test operation mode different from a general operation mode, which can switch an operation mode to the test operation mode by applying to a predetermined external terminal a voltage not smaller than a recommended voltage for the general operation mode.

**Paragraph beginning at line 14 of page 1 has been amended as follows:**

~~Of the semiconductor memory devices, there is one having~~ A conventional semiconductor memory device has a function of switching to ~~the~~ a test operation mode by applying a high voltage to ~~the~~ an external terminal. The high voltage used herein means a voltage beyond a range of a power source voltage applied in the general operation mode. For example, if a maximum operation power source voltage of an integrated

circuit (IC) is 5 V, the voltage higher than 5 V corresponds to the "high voltage"~~; the~~. For example, a high voltage of about 10 V is generally applied.

**Paragraph beginning at line 7 of page 3 has been amended as follows:**

Fig. 3 is a circuit diagram showing a conventional~~, general~~ voltage detection circuit. The circuit is constituted of a pad 31 to which a high voltage is applied for switching the mode to the test operation mode, ~~n~~ an n number of NMOS transistors 32, a resistor 33, and an inverter 34. The NMOS transistors 32 and the resistor 33 are connected in series between the pad 31 and the ground voltage. A high voltage side of the resistor 3 serves as an input terminal of the inverter 34. In this circuit, when the pad 31 is applied with the voltage higher than a total value (n x Vth) of threshold voltages of the NMOS transistors 32 connected in series in n stages, an output level of the inverter 34 is inverted from an H level to an L level, thereby switching the mode to the test operation mode.

**Paragraph beginning at line 13 of page 5 has been amended as follows:**

Further, if ~~increasing~~ the detection voltage is increased, the leak current at the maximum operation voltage

lessens, whereas if ~~decreasing~~ the detection voltage is decreased, the leak current at the maximum operation voltage increases. In other words, to suppress the leak current, the detection voltage should be set as high as possible.

**Heading at line 2 of page 8 has been amended as follows:**

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

**Paragraph beginning at line 16 of page 8 has been amended as follows:**

In the structure of the present invention, the drain region 10 is surrounded by the gate electrode 13, which in this embodiment is formed of a polysilicon layer. With this structure, an electrical isolation between the drain region 10 and an element isolation region is kept with a junction diode functioning as a field effect transistor of the gate electrode 13 at an end in a channel length direction. A uniformity of a current path for a noise or static electricity is achieved, thereby making it possible to increase the drain breakdown voltage.

**Paragraph beginning at line 12 of page 9 has been amended as follows:**

Fig. 5 shows an embodiment to which the present invention is applied. In Fig. 5, a circuit is constituted of

an external terminal 51 to which a high voltage for switching the mode to the test operation mode is applied, a protective transistor 52 connected to the external terminal ~~51,~~ 51 for protecting the IC when ~~being~~ subjected to ~~the~~ electrostatic noise, and a voltage detection circuit 53 for detecting a high voltage for switching ~~the~~ an operation mode to ~~the~~ a test operation mode.

**Paragraph beginning at line 13 of page 10 has been amended as follows:**

The NMOS transistor 54 is constituted of a MOS transistor of a high breakdown voltage, which generally has as high drain junction breakdown voltage ~~as~~ of about 20 V.

**Paragraph beginning at line 22 of page 10 has been amended as follows:**

As set forth above, according to the present invention, ~~the~~ a semiconductor memory device can be ~~provided,~~ provided which suppresses ~~the~~ a terminal leak current in the test operation mode.